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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,693	11/21/2001	Paramjit S. Labana	026473.00004-US	9727

26853 7590 09/28/2004

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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,693	LABANA, PARAMJIT S.	
	Examiner	Art Unit	
	Emerson C Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is made Non-Final. Claims 1-38 have been examined.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

Claim 5-11, 30-34, and 36 objected to because of the following informalities:

In regards to claim 5, the phrase "the first Working Processing Module" lacks antecedent basis.

In regards to claim 5-11, the variable "n" lacks a range of values. Please include a range for variable "n".

In regards to claim 30-34, variables "n" and "i" lack a range of values, please include a range for variables "n" and "i"

In regards to claim 36, the phrase "the terminal Working Processing Module" lacks antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12 and 21-38 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,984,240 of Keren-Zvi et al. referred hereinafter "Keren-Zvi".

In regards to claim 1, Keren-Zvi discloses a protection system comprising:

(i) a plurality of Processing Modules arranged in series comprising at least one Protection Processing Module and at least two Working Processing Modules including a protected Working Processing Module (see figure 3 items 212 and column 6 lines 10-48)

(ii) a signal path comprising

a Normal Path that is connected to the protected Working Processing Module (see figure 3 item 226a)

a Failure Path that is connected to a Processing Module that is logically adjacent to the protected Working Processing Module (see figure 3 item 228a)

(iii) a Protection Bus for connecting the Protection Processing Module to the Processing Module logically adjacent to the protected Working Processing Module (see column 6 lines 42-48)

In regards to claim 2, Keren-Zvi discloses:

wherein the Protection Bus comprises a plurality of Protection Bus Segments, each Protection Bus Segment associated with at least one Working Processing Module (see column 6 lines 42-48)

In regards to claim 3, Keren-Zvi discloses:

wherein, upon failure of the protected Working Processing Module, a connection is formed from the Protection Processing Module to the Failure Path (see column 6 lines 49-58).

In regards to claim 4, Keren-Zvi discloses:

wherein the protected Working Processing Module is not adjacent to the Protection Processing Module (see figure 3 and column 6 lines 49-58)

In regards to claim 5, Keren-Zvi discloses:

for each of i = 1 to n Working Processing Modules (see figure 3 items 212);

an ith signal path comprising

an ith Normal Path that is connected to the ith Working Processing Module (see figure 3 item 226a)

an ith Failure Path that is connected to a Processing Module that is logically adjacent to the ith Working Processing Module (see figure 3 item 228)

wherein the first Working Processing Module is the Working Processing Module that is adjacent to the Protection Processing Module, and the nth Working Processing Module is the Working Processing Module that is logically the farthest Processing Module from the Protection Processing Module (see column 6 line 28-48).

In regards to claim 6, Keren-Zvi discloses

wherein the Protection Bus comprises n-l Protection Bus Segments, and, for i=1 , the ith Protection Bus Segment connects the ith Working Processing Module to the Protection Processing Module, and for i = 2 to n-l, the ith Protection Bus Segment connects the ith Working Processing Module to the (i – l)th Working Processing Module (see column 6 lines 28-58).

In regards to claim 7, Keren-Zvi discloses

wherein for i = 2 to n, upon failure of the ith Working Processing Module, a connection is formed from the Protection Processing Module to the ith Failure Path via the (i – l)th Protection Bus Segment (see column 6 lines 28-58).

In regards to claim 8, Keren-Zvi discloses

wherein the connection formed from the Protection Processing Module to the ith Failure Path further comprises a switching device associated with the (i-l)th Working Processing Module (see figure 3 item 228a).

In regards to claim 9, Keren-Zvi discloses

wherein the connection formed between the Protection Processing Module and the ith Failure Path comprises each Protection Bus Segment logically between the ith Failure Path and the Protection Processing Module (see figure 3 and column 6 lines 28-58).

In regards to claim 10, Keren-Zvi discloses

wherein, for i = 1, upon failure of the ith Working Processing Module a connection is formed from the Protection Processing Module to the ith Failure Path, and the connection does not comprise a Protection Bus Segment associated with a Working Processing Module (see figure 3 and column 6 lines 28-58).

In regards to claim 11, Keren-Zvi discloses

wherein the connection formed between the Protection Processing Module and the ith Failure Path comprises a switching device associated with the Protection Processing Module (see figure 3 item 228a).

In regards to claim 12, Keren-Zvi discloses:

wherein the plurality of Processing Modules comprise at least one switching device for connecting the at least one Protection Bus Segment associated with each of the plurality of Processing Modules to at least one other Protection Bus Segment (see figure 3 item 228a).

In regards to claim 21 and 22, Keren-Zvi discloses:

wherein the plurality of Processing Modules are associated with a backplane, wherein the backplane comprises an electronic circuit board. Keren discloses interface modules including a signal processor, signal processor, fault monitor, and switches (see figure 3 and column 6 lines 28-48), thus it is necessary to have a backplane, wherein the backplane comprises an electronic circuit board, to connection the components.

In regards to claim 23, Keren-Zvi discloses:

wherein the backplane comprises a plurality of slots (see figure 3 and column 6 lines 28-48)

In regards to claim 24, Keren-Zvi discloses:

wherein at least one of the plurality of slots is specially adapted for use with a Network Control Processing Module (see figure 3 item 222 and column 6 lines 28-48).

In regards to claim 25, Keren-Zvi discloses:

wherein the Network Control Processing Module comprises a Distributed Processor Array.(see figure 3 and column 6 lines 28-48)

n-l signal paths, wherein for each of i= 1 to n-l signal paths, the ith signal path comprises an ith Normal Path that is connected to an ith slot, and an ith Failure Path that is connected to a slot that is logically adjacent to the ith slot (see figure 3 and column 6 lines 28-58).

In regards to claim 32, Keren-Zvi discloses:

wherein the Protection Bus comprises n-2 Protection Bus Segments, and, for each of i = 1 to n-2 Protection Bus Segments, the ith Protection Bus Segment connects the ith slot to a slot that is logically adjacent to the ith slot (see figure 3 and column 6 lines 28-58).

In regards to claim 33, Keren-Zvi discloses:

wherein, for i = 2 to n-1, upon failure of a Working Module in the ith slot, a connection is formed from the slot that is logically adjacent to the (i-l)th slot to the ith Failure Path via the (i-l)th Protection Bus Segment (see figure 3 and column 6 lines 28-58).

In regards to claim 34, Keren-Zvi discloses:

wherein the connection formed from the slot that is logically adjacent to the (i-l)th slot to the ith Failure Path further comprises a switching device associated with a Working Processing Module in the (i-l)th slot (see figure 3 and column 6 lines 28-58).

In regards to claim 35, Keren-Zvi discloses:

(i) a plurality of Processing Modules arranged in series comprising at least one Protection Processing Module and at least two Working Processing Modules, wherein at least one Working Processing Module is a protected Working Processing Module, and at least one Working Processing Module is an adjacent Working Processing Module that is logically adjacent to the protected Working Processing Module in the direction of the Protection Processing Module (see figure 3 item 212 and column 6 lines 28-58);

In regards to claim 26, Keren-Zvi discloses:

wherein at least one of the plurality of Processing Modules comprises a Distributed Processor Array (see figure 3 and column 6 lines 28-48).

In regards to claim 27, Keren-Zvi discloses:

(i) a plurality of slots comprising a first slot and a second slot arranged in series, wherein the second slot is logically adjacent to the first slot (see figure 3 item 212);

(ii) a signal path comprising a Normal Path that is connected to the first slot, and a Failure Path that is connected to the second slot (see figure 3 item 226a, 228a) ; and

(iii) a Protection Bus comprising at least one Protection Bus Segment for connecting two adjacent slots (see column 6 lines 42-48).

In regards to claim 28, Keren-Zvi discloses:

wherein the plurality of slots further comprise a third slot (see figure 3 item 212).

In regards to claim 29, Keren-Zvi discloses:

wherein the first, second and third slots are configured to accommodate Processing Modules, and wherein, upon failure of a Processing Module in the first slot, a connection is formed through the Processing Module in the second slot to connect the Failure Path connected to the second slot to a Processing Module in the third slot. (see column 6 lines 49-58).

In regards to claim 30, Keren-Zvi discloses:

wherein the first slot is not logically adjacent to the third slot (see figure 3 and column 6 lines 49-58).

In regards to claim 31, Keren-Zvi discloses:

n slots (see figure 3); and

(ii) for each protected Working Processing Module, a signal path comprising a Normal Path that is connected to the protected Working Processing Module, and a Failure Path that is connected to at least one adjacent Processing Module (see figure 3 item 226a, item 228a); and

(iii) a Protection Bus for connecting the Protection Processing Module to the at least one adjacent Working Processing Module (see column 6 lines 42-48).

In regards to claim 36, Keren-Zvi discloses:

wherein each of the Working Processing Modules except for the terminal Working Processing Module is an adjacent Working Processing Module (see column 6 lines 28-58).

In regards to claim 37, Keren-Zvi discloses:

a plurality of slots for accommodating a plurality of Processing Modules, each of the plurality of Processing Modules capable of performing a service (see column 6 lines 10-18);

a plurality of Protection Bus Segments, each Protection Bus Segment capable of forming a connection between two adjacent slots (see column 6 lines 42-48);

means for forming a Protection Group comprising a plurality of Processing Modules capable of being interconnected in series by a plurality of the plurality of Protection Bus Segments, where the plurality of Processing Modules is fewer than the plurality of slots (see figure 3 and column 6 lines 42-48); and

means for designating a Protection Processing Module within the Protection Group, such that upon failure of a Processing Module in the Protection Group other than the Protection Processing Module, the Protection Processing Module becomes capable of performing the service provided by the failed Processing Module (see column 6 lines 59-68).

In regards to claim 38, Keren-Zvi discloses:

(i) providing at least one Protection Group comprising a Protection Processing Module and at least one Working Processing Module comprising a first Working Processing Module (see figure 3 item 212 and column 6 lines 10-48);

(ii) providing a segmented Protection Bus operatively linking the Protection Processing Module and the at least one Working Processing Module (see column 6 lines 42-48); and

(iii) providing a signal path comprising a Normal Path that can be connected to the first Working Processing Module and a Failure Path that can be connected to a Processing Module that is logically adjacent to the first Working Processing Module (see figure 3 items 226a,228a,) wherein upon failure of the first Working Processing Module, a connection is formed from the Protection Processing Module to the Failure Path connected to the Processing Module that is logically adjacent to the first Working Processing Module (see figure 3 and column 6 lines 49-58)..

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13 and 14 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over Keren-Zvi in view of US Patent No. 6,271,605 of Carkner et al. referred hereinafter "Carkner".

In regards to claim 13 and 14, Keren-Zvi fails to discloses:

wherein the at least one switching device comprises at least one electromechanical switching device or wherein the at least one switching device comprises at least one optical switching device.

However Keren-Zvi discloses a switching device (see figure 3 item 226a and column 6 lines 19-26)

Carkner disclose known types of switching devices including electromechanical switches and electro-optical switch, indicating a optical switch.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an electromechanical switches or a optical switch. A person of ordinary skill in the art at the time of the invention would have been motivated because Keren-Zvi discloses a switching device and electromechanical switches or a optical switch are well know switching devices, as per teaching of Carkner.

Claims 15-20 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over Keren-Zvi.

In regards to claim 15, Keren-Zvi primary teaching fails to disclose:

means for configuring the plurality of Processing Modules into a plurality of Protection Groups, each Protection Group comprising at least one Working Processing Module and at least one Protection Processing Module.

However, Keren-Zvi discloses a secondary teaching wherein assigning a partner module (see figure 1 and column 3 lines 5-10), indicating a plurality of protection groups.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configuring the plurality of Processing Modules into a plurality of Protection Groups, each Protection Group comprising at least one Working Processing Module and at least one Protection Processing Module. A person of ordinary skill in the art at the time of the invention would have been motivated because Keren-Zvi primary teaching provides a redundant module for interfacing with communication lines in case of failure of a primary interface module and the secondary teaching is alternate method using pairs/partner to provide a redundant module for interfacing with communication lines in case of failure of a primary interface module

In regards to claim 16, Keren-Zvi discloses:

wherein the configuring means comprises a Network Control Processing Module (see figure 3 item 232).

In regards to claim 17, Keren-Zvi discloses:

wherein the configuring means comprises at least one switching device (see figure 3 item 226a).

In regards to claim 18, Keren-Zvi secondary teaching discloses:

wherein the plurality of Processing Modules are configured into a plurality of Protection Groups, each Protection Group comprising at least one Working Processing Module and at least one Protection Processing Module. Keven Zvi discloses assigning a partner module, indicating a plurality of protection groups (see figure 1 and column 3 lines 5-10),

In regards to claim 19, Keren-Zvi discloses,

wherein the configuring means comprises a Distributed Processor Array (see figure 3).

In regards to claim 20, Keren-Zvi discloses:

wherein the Distributed Processor Array comprises at least one of the plurality of Processing Modules (see figure 3).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (703) 305-8012. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-5631.

Emerson Puente
9/22/04

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

PTO/SB/08a/b (06-03)
Approved for use through 07/31/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/989,693-Conf. #9727
Filing Date	November 21, 2001
First Named Inventor	Paramjit S. Labana
Art Unit	2184
Examiner Name	R. Beausoliel
Attorney Docket Number	026473.00004-US01

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
EP	CA	Synchronous Optical Network (SONET)-Automatic Protection Switching, American National Standards Institute T1.105.01 (1998).	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	Emerson Puente	Date Considered	9/20/04

Notice of References Cited	Application/Control No. 09/989,693	Applicant(s)/Patent Under Reexamination LABANA, PARAMJIT S.	
	Examiner Emerson C Puente	Art Unit 2113	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-4,984,240	01-1991	Keren-Zvi et al.	714/4
	B	US-6,271,605	08-2001	Carkner et al.	307/125
	C	US-6,792,558	09-2004	Kuwako et al.	714/13
	D	US-6,615,362	09-2003	Daruwalla et al.	714/4
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	O					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.